CLAIMS

What is claimed is:

1. A fabrication method, comprising the steps of:
(a) providing a substrate which includes at least one substantially monolithic body of semiconductor material;
(b) forming n-type and p-type regions at a surface of said body;
(c) forming an oxidation barrier layer on said surface;
(d) forming a first patterned layer which exposes predetermined locations of isolation areas in said n-type region, and which covers substantially all of said p-type regions and predetermined locations of active device areas in said n-type regions; and thereafter
(d.1) etching away said oxidation barrier layer where exposed by said respective patterned layer, and
(d.2) implanting a first channel-stop dopant into areas exposed by said respective patterned layer, and
(d.3) removing said respective patterned layer;
(e) forming a second patterned layer which exposes predetermined locations of isolation areas in said p-type region, and which covers substantially all of said n-type regions and predetermined locations of active device areas in said p-type regions; and thereafter
(e.1) etching away said oxidation barrier layer where exposed by said respective patterned layer, and
(e.2) implanting a second channel-stop dopant into areas exposed by said respective patterned layer, and
(e.3) removing said respective patterned layer; and
(f) growing a field oxide on said body where exposed by said oxidation barrier layer.

2. The method of Claim 1, wherein said step (e) is performed before said step (d).

3. The method of Claim 1, wherein said step (d) is performed before said step (e).

4. The method of Claim 1, wherein said body consists of silicon.

5. The method of Claim 1, wherein said first channel-stop dopant consists of phosphorus.

6. The method of Claim 1, wherein said second channel-stop dopant consists of boron.

7. The method of Claim 1, wherein said oxidation barrier layer comprises a layer of silicon nitride overlying a layer of silicon dioxide.

8. The method of Claim 1, wherein said oxidation barrier layer comprises a silicon oxide layer, a polycrystaline silicon layer thereover, and a layer of silicon nitride thereover.

9. The method of Claim 1, wherein said oxidation barrier layer comprises a first layer of silicon nitride overlying a silicon oxide layer which overlies a second silicon nitride layer.

10. The method of Claim 1, further comprising the subsequent steps of forming active devices in at least some ones of said active areas, and forming interconnections to link said active devices in a predetermined circuit configuration.

11. A fabrication method, comprising the steps of:

(a) providing a substrate which includes at least one substantially monolithic body of semiconductor material;

(b) forming n-type and p-type regions at a surface of said body;

(c) forming an oxidation barrier layer on said surface;

(d) forming a first patterned layer which exposes predetermined locations of isolation areas in said n-type region, and which covers substantially all of said p-type regions and predetermined locations of active device areas in said n-type regions; and thereafter

(d.1A) etching away said oxidation barrier layer where exposed by said respective patterned layer, and

(d.1B) etching away said body where exposed by said oxidation barrier layer, and

(d.2) implanting a first channel-stop dopant into exposed areas of said body, and

(d.3) removing said respective patterned layer;

(e) forming a second patterned layer which exposes predetermined locations of isolation areas in said p-type region, and which covers substantially all of said n-type regions and predetermined locations of active device areas in said p-type regions; and thereafter

(e.1A) etching away said oxidation barrier layer where exposed by said respective patterned layer, and

(e.1B) etching away said body where exposed by said oxidation barrier layer, and

(e.2) implanting a second channel-stop dopant into exposed areas of said body, and

(e.3) removing said respective patterned layer; and

(f) growing a field oxide on said body where exposed by said oxidation barrier layer.

12. The method of Claim 11, wherein said step (e) is performed before said step (d).

13. The method of Claim 11, wherein said step (d) is performed before said step (e).

14. The method of Claim 11, wherein said body consists of silicon.

15. The method of Claim 11, wherein said first channel-stop dopant consists of phosphorus.

16. The method of Claim 11, wherein said second channel-stop dopant consists of boron.

17. The method of Claim 11, wherein said oxidation barrier layer comprises a layer of silicon nitride overlying a layer of silicon dioxide.

18. The method of Claim 11, wherein said oxidation barrier layer comprises a silicon oxide layer, a polycrystaline silicon layer thereover, and a layer of silicon nitride thereover.

19. The method of Claim 11, wherein said oxidation barrier layer comprises a first layer of silicon nitride overlying a silicon oxide layer which overlies a second silicon nitride layer.

20. The method of Claim 11, further comprising the subsequent steps of forming active devices in at least some ones of said active areas, and forming interconnections to link said active devices in a predetermined circuit configuration.

21. A method, comprising the steps of:

(a) providing a substrate which includes at least one substantially monolithic body of semiconductor material;

(b) forming n-type and p-type regions at a surface of said body;

(c) forming an oxidation barrier layer on said surface;

(d) forming a first patterned layer which exposes predetermined locations of isolation areas in said n-type region, and which covers substantially all of said p-type regions and predetermined locations of active device areas in said n-type regions; and thereafter

(d.1) etching away said oxidation barrier layer where exposed by said respective patterned layer, and

(d.2) implanting a first channel-stop dopant into areas exposed by said respective patterned layer, and

(d.3) removing said respective patterned layer;

(e) forming a second patterned layer which exposes predetermined locations of isolation areas in said p-type region, and which covers substantially all of said n-type regions and predetermined locations of active device areas in said p-type regions; and thereafter

(e.1) etching away said oxidation barrier layer where exposed by said respective patterned layer, and

(e.2) implanting a second channel-stop dopant into areas exposed by said respective patterned layer, and

(e.3) removing said respective patterned layer; and

(f.1) depositing and partially removing an additional layer of oxidation-resistant material; and

(f.2) growing a field oxide on said body where exposed by said oxidation barrier layer.

22. The method of Claim 21, wherein said step (e) is performed before said step (d).

23. The method of Claim 21, wherein said step (d) is performed before said step (e).

24. The method of Claim 21, wherein said body consists of silicon.

25. The method of Claim 21, wherein said first channel-stop dopant consists of phosphorus.

26. The method of Claim 21, wherein said second channel-stop dopant consists of boron.

27. The method of Claim 21, wherein said oxidation barrier layer comprises a layer of silicon nitride overlying a layer of silicon dioxide.

28. The method of Claim 21, wherein said oxidation barrier layer comprises a silicon oxide layer, a polycrystaline silicon layer thereover, and a layer of silicon nitride thereover.

29. The method of Claim 21, wherein said additional oxidation-resistant material consists of silicon nitride.

30. The method of Claim 21, wherein said oxidation barrier layer comprises a first layer of silicon nitride overlying a silicon oxide layer which overlies a second silicon nitride layer.

31. The method of Claim 21, further comprising the subsequent steps of forming active devices in at least some ones of said active areas, and forming interconnections to link said active devices in a predetermined circuit configuration.